(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 December 2001 (27.12.2001)

PCT

(10) International Publication Number
WO 01/98853 A1

(51) International Patent Classification[7]: G05F 1/00, H05B 37/02

(21) International Application Number: PCT/US01/19406

(22) International Filing Date: 18 June 2001 (18.06.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/212,643 19 June 2000 (19.06.2000) US

(71) Applicant: INTERNATIONAL RECTIFIER CORPORATION [US/US]; 233 Kansas Street, El Segundo, CA 90245 (US).

(72) Inventor: RIBARICH, Thomas, J.; 2470 South Coast Highway, Apartment D, Laguna Beach, CA 92651 (US).

(74) Agents: WEINER, Samuel, H. et al.; Ostrolenk, Faber, Gerb & Soffen, LLP, 1180 Avenue of the Americas, New York, NY 10036 (US).

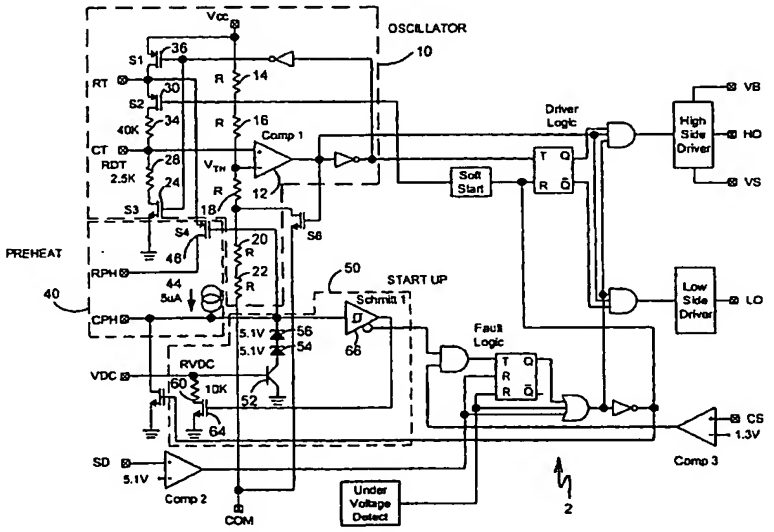
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

[Continued on next page]

(54) Title: BALLAST CONTROL IC WITH MINIMAL INTERNAL AND EXTERNAL COMPONENTS



(57) Abstract: A ballast controller integrated circuit which executes a specific set of instructions via an integrated state diagram architecture to control a fluorescent lamp or high intensity discharge lamp and protect the ballast. The state diagram architecture (Fig. 2) controls powering up and down of the IC (2) and the half-bridge circuit (6, 8) driven by the IC (2), preheating and striking of the lamp (4), running of the lamp (4), sensing for numerous possible fault conditions, and recovering from these fault conditions based on the normal maintenance of the lamp (4), while requiring fewer internal and external components than previous electronic ballasts.

WO 01/98853 A1

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

BALLAST CONTROL IC WITH MINIMAL INTERNAL AND EXTERNAL COMPONENTS

BACKGROUND OF THE INVENTION

1. Field of the Invention:

The present invention relates to an electronic ballast for controlling fluorescent or high-intensity discharge lamps, and more particularly, to an electronic ballast that requires fewer internal and external components.

2. Description of the Related Art:

Electronic ballasts for controlling fluorescent or high-intensity discharge (HID) lamps usually require electronics necessary for preheating the lamp filaments, striking the lamp, driving the lamp to a given power, detecting lamp fault conditions, and safely deactivating the circuit.

Electronic ballasts for gas discharge circuits have recently come into widespread use because of the availability of power MOSFET switching devices and insulated gate bipolar transistors ("IGBTs") that can replace previously used power bipolar switching devices. Monolithic gate driver circuits, such as the IR2155 sold by International Rectifier Corporation and described in U.S. Pat. No. 5,545,955, the disclosure of which is incorporated herein by reference in its entirety, have been devised for driving the power MOSFETs or IGBTs in electronic ballasts.

The IR2155 gate driver IC offers significant advantages over prior circuits: The driver is packaged in a conventional DIP or SOIC package. The package contains internal level shifting circuitry, under voltage lockout circuitry, deadtime delay circuitry, and additional logic circuitry and inputs so that the driver can self-oscillate at a frequency determined by external resistors R_T and capacitors C_T.

Although the IR2155 offers a vast improvement over prior ballast control circuits, it lacks a number of desirable features such as the following: (i) a

start-up procedure which ensures a flash-free start without an initial high voltage pulse across the lamp, (ii) non-zero voltage switching protection circuitry, (iii) over-temperature shutdown circuitry, (iv) DC bus and AC on/off control circuitry, and (v) near or below resonance detection circuitry.

U.S. Pat. No. 6,211,623 to Wilhelm et al. issued April 3, 2001 and having common assignment with the present application discloses an electronic ballast which addresses limitations of the IR2155, such as those discussed above. The electronic ballast is identified by the assignee, International Rectifier Corporation, as the IR2157.

The ballast control circuit of the '623 patent, as in commonly known ballasts, requires an implementation of the preheat timer that includes a comparator for comparing the CPH pin against a fixed threshold. In addition, the oscillator circuit requires more than one comparator. These and other configuration details result in additional components being required both inside and outside the chip. Accordingly, the prior art could be improved upon by providing a ballast control IC which performs the primary ballast functions while minimizing the internal and external component count. Applications for such ballasts would include linear fluorescent lamps, compact fluorescent lamps (CFL), cold-cathode fluorescent lamps (CCFL), high-intensity discharge (HID) lamps, and flat fluorescent lamps.

SUMMARY OF THE INVENTION

The present invention overcomes the deficiencies of the prior art, such as those described above, by providing an electronic ballast that utilizes fewer comparators and combines the functionality of sub-circuits, thereby reducing the number of internal and external components required.

More specifically, the chip of the present invention includes an oscillator circuit that advantageously requires only one comparator circuit. In addition, a lamp preheat circuit uses a preheat resistor parallel to the timing resistor to program preheat frequency, and the voltage at the gate of a MOSFET switch is ramped to gradually disconnect the preheat pin (and thus the preheat resistor)

from the frequency timing input. Also, the preheat circuit ramp is utilized as a ramp for lamp ignition as well, thus saving on circuit components. Further, the preheat capacitor input is used as a convenient delay for connecting a DC bus sensing resistor to a DC bus sensing input.

The integrated circuit of the present invention includes circuitry for performing the following functions: micro-power start-up current, programmable preheat frequency, programmable ignition-current or over-current, programmable preheat time, programmable ignition ramp, programmable running or minimum frequency, programmable dead-time, programmable low DC bus frequency-shift reset, external shutdown pin, and high-and low-side 600V half-bridge driver outputs for driving two MOSFETs or IGBTs connected in a classic totem-pole configuration.

Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a state diagram showing the functionality incorporated into a ballast control integrated circuit according to the present invention.

Fig. 2 is a typical connection diagram for driving a single fluorescent lamp with the ballast control circuit of the present invention.

Fig. 3 illustrates a basic block diagram of the ballast control circuit of the present invention.

Fig. 4 is a detailed schematic of oscillator circuitry of the integrated ballast control circuit according to the present invention

Fig. 5 is a schematic illustration of preheat circuitry according to a preferred embodiment of the present invention.

Fig. 6 is a schematic diagram of start-up and low DC bus frequency-shift reset circuitry of the integrated ballast control circuit of the present invention.

Fig. 7 is a timing diagram for the ballast control circuit of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

Overview:

Referring first to Fig. 1, a state diagram is shown that is incorporated into the operation of the integrated circuit (IC) **2** of the present invention for controlling an electronic (rapid start) fluorescent lamp ballast. Fig. 2 illustrates a typical connection diagram for driving a single fluorescent lamp **4** with the integrated circuit **2** of the present invention. Fig. 3 illustrates a basic block diagram of the integrated circuit **2** of the present invention. Many of the aspects of the present invention shown in Figs. 1-3 are similar to the disclosure of U.S. Pat. No. 6,211,623 to Wilhelm et al. issued April 3, 2001 and incorporated herein by reference, and will be discussed further below. However, significant aspects and advantages of the present invention, particularly with respect to oscillator **10**, preheat circuit **40** and start-up circuit **50** shown in Fig. 3, will be discussed, as follows:

Oscillator:

Fig. 4 is a detailed schematic of oscillator circuit **10** according to the present invention. In contrast to prior ballast ICs, the oscillator circuit advantageously requires only one comparator **12** and therefore significantly reduces the layout space required for implementation into silicon. Accordingly, the overall size of the IC can be reduced.

Operationally, the minus (-) input of comparator **12**, Vth, initially is at $^3/_5$ VCC, which is established by the voltage divider formed by five resistors **14**, **16**, **18**, **20**, and **22** of equal resistance connected in series between VCC and COM. The on/off control signal $\overline{\text{ENABLE}}$ is a logic 'high', therefore turning MOSFET **24** 'on' which keeps the timing capacitor C_T discharged to COM through dead-time resistor **28**. Pin CT serves as the plus (+) input of comparator **12** and is initially at COM, therefore the output of comparator **12** is a logic 'low.'

Switch **30** is 'off' initially due to the output of OR gate **32** being 'high' when $\overline{\text{ENABLE}}$ is 'high.' Pin RT is therefore at the same potential as pin CT due to their connection through timing resistor R_T. Once $\overline{\text{ENABLE}}$ goes 'low'

(see Timing Diagram, Fig. 7), MOSFET switch **24** is 'opened' and switch **30** is 'closed'. As a result, timing capacitor C_T charges exponentially towards VCC through timing resistor R_T at a rate given by the following equation:

$$v_{CT}(t) = VCC(1 - e^{-t/RC})$$

where,

R = resistance of timing resistor R_T	[Ohms]
C = capacitance of timing capacitor C_T	[Farads]
t = time	[Seconds]

When the voltage on pin CT exceeds $^3/_5$ VCC, the output of comparator **12** goes 'high' causing switch **36** to 'close,' switch **30** to 'open,' and switch **24** to 'close.' Timing capacitor C_T then discharges exponentially towards COM through dead-time resistor **28** at a rate given by:

$$v_{CT}(t) = (^3/_5\, VCC)e^{-t/RC}$$

Closing switch **36** changes the threshold at pin CT from $^3/_5$ VCC to ⅓ VCC. In doing so, inherent positive feedback forces the comparator output to transition quickly with a single edge. When capacitor C_T discharges below ⅓ VCC, the output of comparator **12** goes 'low' again, and the cycle repeats itself.

This charging and discharging of CT between $^3/_5$ VCC and ⅓ VCC continues indefinitely until the $\overline{\text{ENABLE}}$ signal goes once again 'high'.

During steady state oscillations, the charging and discharge times are given as:

Charging: $$v_{CT}(t) = \left(VCC - {}^1/_3\, VCC\right)\left(1 - e^{-t/RC \cdot CT}\right)$$

Discharging: $$v_{CT}(t) = {}^3/_5\ VCC\ e^{-t/RT \cdot CT}$$

The charging time determines the 'on' time of gate drive signals HO and LO (see Timing Diagram, Fig. 7). The discharge time determines the dead-time between

gate drive signals HO and LO (see Timing Diagram, Fig. 7). This preferred oscillator of the present invention results in less circuitry than oscillator circuits of previous ballast ICs, specifically requiring only one comparator. The oscillator is ratiometric with VCC and is therefore independent of VCC. The threshold values selected are arbitrary.

Preheat Timer and Ignition Ramp

Fig. 5 is a schematic illustration of preheat circuit **40** according to a preferred embodiment of the present invention. Advantageously, preheat circuit **40** does not require any comparators.

During preheat, it is necessary for the IC to oscillate at a higher preheat frequency. This is followed by a smooth downward sweep through the ignition frequency to the final running or minimum frequency. To do this, an external capacitor C_{PH} is charged linearly from COM to VCC through an internal 5μA current source **44** flowing out of the CPH pin. The CPH pin is also connected to the gate of a PMOS transistor **46** which connects pin RPH to pin RT. In this configuration, resistor R_T is connected in parallel with resistor R_{PH} such that the oscillator frequency is higher during preheat. Since the threshold of the PMOS is about 1.5 volts, the preheat period is defined as the time it takes for capacitor C_{PH} to ramp from COM to (VCC - 1.5 volts). As capacitor C_{PH} continues to charge from (VCC - 1.5V) to VCC, switch **46** opens slowly, which slowly disconnects pin RPH from RT. This causes the frequency to transition slowly from the preheat frequency to the final running frequency. (See Timing Diagram, Fig.7).

The advantageous features of preheat circuit **40** are: 1) using a resistor R_{PH} parallel to resistor R_T to program the preheat frequency; 2) ramping the voltage at the gate of PMOS **46** to disconnect the RPH pin smoothly from the RT pin; and 3) using the existing capacitor C_{PH} ramp as the ramp for ignition as well. Classical implementation of the preheat timer requires a comparator for comparing the CPH pin against a fixed threshold. By combining the above-noted

three functions in preheat circuit **40** of the present invention, a 'comparator-less' pre-heat timer is realized, thereby reducing the overall size of the IC.

Start-up Circuitry and Low DC Bus Frequency-Shift Reset:

Start-up and low DC bus frequency-shift reset circuitry **50** is shown in the schematic of Fig. 6. The circuit senses the DC bus and properly resets the circuit back to preheat mode if the DC bus decreases below a level where the lamp can extinguish. Failure to do this can result in the lamp extinguishing during a brown-out line condition and not being re-ignited when the AC input returns. Decreasing the DC bus also can cause hard-switching at the half-bridge output which can damage or destroy the power MOSFETs or IGBTs. It is therefore convenient to increase the frequency as the DC bus decreases such that the ballast operating point always remains above resonance and no hard-switching occurs.

Circuit **50** of the present invention achieves this by using the VDC pin to sense the DC bus. If VDC decreases below (VCC-10.9V), the CPH pin is pulled down linearly with the VDC pin. This gradually will re-connect RPH with RT and therefore gradually shift the frequency higher.

The 10.9V threshold is achieved with a PNP transistor **52**, and the two 5.1 zener diodes **54** and **56**, connected in series. The base of transistor **52** is connected to pin VDC, the collector of transistor **52** is connected to COM, and the emitter is connected to the anode of the lower diode **54**. The cathode of the upper diode is then connected to pin CPN. In this configuration, the frequency is not increased until VDC goes below the two zener voltages (10.2V) plus the emitter-to-base voltage of transistor **52** ($\simeq$ 0.7) = 10.9V. Fig. 8 depicts this graphically.

To program the DC bus level at which the frequency shift occurs, an external resistor **58** (R_{SUPPLY}), with an internal resistor **60**, form a voltage divided ratio of the DC bus at pin VDC. To further reduce external component count,

resistor **58** also supplies micro-power start-up current to the IC. As the DC bus increases at ballast turn-on, current flows from the DC bus, through the resistor **58**, into pin VDC, through the existing ESD diode **62** connected between VDC and VCC.

Once VCC exceeds the positive-going under-voltage lock-out threshold, UVLO (+), an external charge pump (or other form of supply) connected to VCC through an external diode **63** takes over as the supply for VCC and increases VCC up to the internal zener clamp voltage (see Timing Diagram, Fig.7). Resistor **60** then is connected internally to pin VDC through MOSFET **64** when CPH exceeds the threshold voltage (≃ ½ VCC) of Schmitt trigger **66**. This occurs at approximately half way through the preheat time. The CPH pin is used as a convenient delay for connecting RVDC to pin VDC, which also contributes to reducing the overall size of the IC.

State Diagram

Referring back now to Fig. 1, the integrated circuit **2** of the present invention advantageously executes a very specific set of instructions to control the lamp **4** and protect the ballast. The IC accurately controls and properly performs the functions of: powering up and down the IC **2** and the half-bridge (MOSFETs **6** and **8**); preheating and striking the lamp; running the lamp; sensing for numerous possible fault conditions; and recovering from these fault conditions based on normal lamp maintenance.

The state machine operates between five basic modes of operation based on the status of the various inputs to the IC. These five modes of operation include:

1) under voltage lockout mode;
2) preheat mode;
3) ignition ramp mode;
4) run mode; and
5) fault mode.

Fig. 2 illustrates the pinouts of the IC **2**, including all of its inputs and outputs. The inputs to the chip include:

1) VCC
2) VDC
3) SD
4) CS
5) CPH
6) CT
7) RT

VCC represents both an input to be sensed and the primary low voltage supply to the IC. In addition to these seven inputs, the IC surface junction temperature represents an eighth input. The outputs of the IC include:

1) HO
2) LO
3) RPH
4) RUN
5) DT

The supplies to the IC include:

1) VCC
2) COM
3) VB
4) VS

The general description for the IC functions of the present invention are as follows:

Under-voltage Lock-Out Mode (UVLO)

The under-voltage lock-out mode (UVLO) is defined as the state the IC is in when VCC is below the turn-on threshold of the IC. The undervoltage lock-out is designed to maintain an ultra low supply current of less than 150uA, and to guarantee the IC is fully functional before the high and low side output drivers are activated. Fig. 1 shows an efficient supply voltage using the start-up current

of the ballast IC together with a charge pump from the ballast output stage (resistor **58**, capacitors **70, 72**, D_{CP1} and D_{CP2}).

The start-up capacitors **70, 72** (C_{VCC}) are charged by current through supply resistor **58** (R_{SUPPLY}) minus the start-up current drawn by the IC. Resistor **58** is connected to VCC internally through a diode, and is chosen to fulfill two functions. The first is to provide twice the maximum start-up current to guarantee ballast start-up at low line input voltage. The second is to set the IC reset threshold in case of a decreasing DC bus (described in more detail above). Once the capacitor voltage on VCC reaches the start-up threshold, and the SD pin is below 4.5 volts, the IC turns on and HO and LO begin to oscillate. Capacitors **70, 72** begin to discharge due to the increase in IC operating current.

During the discharge cycle, the rectified current from the charge pump charges the capacitor above the IC turn-off threshold. The charge pump and the internal 15.6V zener clamp of the IC take over as the supply voltage. The start-up capacitors **70, 72** and snubber capacitor **80** must be selected such that enough supply current is available over all ballast operating conditions. A bootstrap diode **82** and supply capacitor **84** comprise the supply voltage for the high side driver circuitry. To guarantee that the high-side supply is charged up before the first pulse on pin HO, the first pulse from the output drivers comes from the LO pin. During undervoltage lock-out mode, the high- and low-side driver outputs HO and LO are both low, pin CT is connected internally to COM to disable the oscillator, and pin CPH is connected internally to COM for resetting the preheat time.

Preheat Mode (PH)

The preheat mode is defined as the state the IC is in when the lamp filaments are being heated to their correct emission temperature. This is necessary for maximizing lamp life and reducing the required ignition voltage. The ballast control IC enters preheat mode when VCC exceeds the UVLO

positive-going threshold. HO and LO begin to oscillate at the preheat frequency with 50% duty cycle and with a dead-time which is set by the value of the external timing capacitor C_T, and internal deadtime resistor, RDT. Pin CPH is disconnected from COM and an internal 1uA current source (Fig. 3) charges the external preheat time capacitor on CPH linearly. The over-current protection on pin CS is disable during preheat. The preheat frequency is determined by the parallel combination of resistors R_{PH} and R_T, together with timing capacitor C_T. Capacitor C_T charges and discharges between ⅓ and $^3/_5$ of VCC (see Timing Diagram, Fig. 7). C_T is charged expontentially through the parallel combination of R_T and R_{PH} connected internally to VCC through MOSFET **36**. The charge time of C_T from ⅓ and $^3/_5$ VCC is the on-time of the respective output gate driver, HO or LO. Once CT exceeds $^3/_5$ VCC, MOSFET **36** is turned off, disconnecting RT and RPH from VCC. Capacitor C_T then is discharged exponentially through an internal resistor, RDT, through MOSFET **24** to COM. The discharge time of timing capacitor C_T from $^3/_5$ to ⅓ VCC is the dead-time (both off) of the output gate drivers, HO and LO. The selected values of capacitor C_T together with RDT (resistor **28**) therefore program the desired dead-time (see Design Equations 1 and 2). Once capacitor C_T discharges below ⅓ VCC, MOSFET **24** is turned off, disconnecting RDT from COM, and MOSFET **36** is turned on, connecting RT and RPH again to VCC. The frequency remains at the present frequency until the voltage on pin CPH exceeds 13V and the IC enters Ignition Mode. During the preheat mode, both the over-current protection and the DC bus under-voltage reset are enabled when pin CPH exceeds 7.5V.

Ignition Mode (IGN)

The ignition mode is defined as the state the IC is in when a high voltage is being established across the lamp necessary for igniting the lamp. The ballast control IC enters ignition mode when the voltage on pin CPH exceeds 13V.

Pin CPH is connected internally to the gate of a p-channel MOSFET **46** of preheat circuit **40** (see Fig. 5) that connects pin RPH with pin RT. As pin CPH exceeds 13V, the gate-to-source voltage of MOSFET **46** begins to fall below the

turn-on threshold of MOSFET **46**. As pin CPH continues to ramp towards VCC, MOSFET switch **46** turns off slowly. This results in preheat resistor R_{PH} being disconnected smoothly from timing resistor R_T, and therefore causing the operating frequency to ramp smoothly from the preheat frequency, through the ignition frequency, to the final run frequency. The over-current threshold on pin CS will protect the ballast against a non-strike or open-filament lamp fault condition. The voltage on pin CS is defined by the lower half-bridge MOSFET current flowing through the external current sensing resistor R_{CS}. Current sensing resistor R_{CS} therefore programs the maximum allowable peak ignition current (and therefore peak ignition voltage) of the ballast output stage. The peak ignition current must not exceed the maximum allowable current ratings of the output stage MOSFETs. If this voltage exceeds the internal threshold of 1.3V, the IC will enter FAULT mode and both gate driver outputs HO and LO will be latched low.

Run Mode (RUN)

Once the lamp has successfully ignited, the ballast enters the run mode. The run mode is defined as the state the IC is in when the lamp arc is established and the lamp is being driven to a given power level. The run mode oscillating frequency is determined by the timing resistor R_T and timing capacitor C_T (see Design Equations 3 and 4 in the following section). Should hard-switching occur at the half-bridge at any time due to an open-filament or lamp removal, the voltage across the current sensing resistor R_{CS} will exceed the internal threshold of 1.3 volts and the IC will enter FAULT mode. Both gate driver outputs, HO and LO, will be latched low.

DC Bus Under-voltage Reset:

If the voltage of the DC bus decreases too far during a brown-out line condition or over-load condition, the resonant output stage to the lamp can shift near or below resonance. This can produce hard-switching at the half-bridge which can damage the half-bridge switches. To protect against this, pin VDC

measures the DC bus voltage and pulls down on pin CPH linearly as the voltage on pin VDC decreases 10.9V below VCC. This causes the p-channel MOSFET **46** (Fig. 4) to close as the DC bus decreases and the frequency to shift higher to a safe operating point above resonance. The DC bus level at which the frequency shifting occurs is set by the external resistor **58** and internal RVDC resistor. By pulling down on pin CPH, the ignition ramp is also reset. Therefore, should the lamp extinguish due to very low DC bus levels, the lamp will be automatically ignited as the DC bus increases again. The internal RVDC resistor is connected between pin VDC and COM when CPH exceeds 7.5V (during preheat mode). This allows for resistor **58** to serve also as the start-up resistor for the IC, therefore minimizing component count.

Fault Mode (FAULT)

If the voltage at the current sensing pin, CS, exceeds 1.3 volts at any time after the preheat mode, the IC enters fault mode and both gate driver outputs, HO and LO, are latched in the 'low' state. CPH is discharged to COM to reset the preheat time, and CT is discharged to COM for disabling the oscillator. To exit the fault mode, VCC must be recycled back below the UVLO negative-going turn-off threshold, or, the shutdown pin, SD, must be pulled above 5.1 volts. Either of these conditions will force the IC to enter UVLO mode (see State Diagram, page 2). Once VCC is above the turn-on threshold and SD is below 4.5 volts, the IC will begin oscillating again in the preheat mode.

Design Equations

The design equations for implementing the ballast IC of the present invention are as follows:

Step 1: Program Dead-time

The dead-time between the gate driver outputs HO and LO is programmed with timing capacitor C_T and internal dead-time resistor **28** (see Fig.

4). The dead-time is the discharge time of capacitor C_T from $^3/_5$ VCC to ⅓ VCC and is given as:

$$t_{DT} = C_T \cdot 1475 \quad \text{[Seconds]} \quad (1)$$

or

$$C_T = \frac{t_{TD}}{1475} \quad \text{[Farads]} \quad (2)$$

Step 2: Program Run Frequency

The final run frequency is programmed with timing resistor R_T and timing capacitor C_T. The charge time of capacitor C_T from ⅓ VCC to $^3/_5$ VCC determines the on-time of HO and LO gate driver outputs. The run frequency is therefore given as:

$$f_{RUN} = \frac{1}{2.C_T(0.51.R_T + 1475)} \quad \text{[Hertz]} \quad (3)$$

or

$$R_T = \frac{1}{1.02 \cdot C_T \cdot f_{RUN}} - 2892 \quad \text{[Ohms]} \quad (4)$$

Step 3: Program Preheat Frequency

The preheat frequency is programmed with timing resistor R_T and preheat resistor R_{PH} and timing capacitor C_T. Timing resistor R_T and preheat resistor R_{PH} are connected in parallel internally for the duration of the preheat time. The preheat frequency is therefore given as:

$$f_{PH} = \frac{1}{2 \cdot C_T \cdot \left(\frac{0.51 \cdot R_T \cdot R_{PH}}{R_T + R_{PH}} + 1475\right)} \quad \text{[Hertz]} \quad (5)$$

or

$$R_{PH} = \frac{\left(\frac{1}{1.02 \cdot C - \cdot f_{PH}} - 2892\right) \cdot R_T}{R_T - \left(\frac{1}{1.02 \cdot C_T \cdot f_{PH}} - 2892\right)} [\text{Ohms}] (6)$$

Step 4: Program Preheat Time

The preheat time is defined by the time it takes for capacitor C_{PH} on pin CPH to charge up to 13 volts. An internal current source of 5μA flows out of pin CPH. The preheat time is therefore given as:

$$t_{PH} = C_{PH} \cdot 2.6e6 \qquad [\text{Seconds}] \quad (7)$$

or

$$C_{PH} = t_{PH} \cdot 0.385e-6 \qquad [\text{Farads}] \quad (8)$$

Step 5: Program Maximum Ignition Current

The maximum ignition current is programmed with the external resistor RCS and an internal threshold of 1.3 volts. This threshold determines the over-current limit of the ballast, which can be exceeded when the frequency ramps down towards resonance during ignition and the lamp does not ignite. The maximum ignition current is given as:

$$I_{IGN} = \frac{1.3}{R_{CS}} \qquad [\text{Amps Peak}] \quad (9)$$

or

$$R_{CS} = \frac{1.3}{I_{IGN}} \qquad [\text{Ohms}] \quad (10)$$

Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses

will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

WHAT IS CLAIMED IS:

1. An integrated circuit for providing an oscillating signal in accordance with the charging and discharging of a capacitor, comprising:

comparator circuitry for comparing the voltage across the capacitor to a reference voltage and generating a charge/discharge signal in response to the value of the voltage across the capacitor as compared to the reference voltage, wherein the reference voltage is switched between at least two values comprising a first reference voltage and a second reference voltage, and wherein the charge/discharge signal has a first binary value when the voltage across the capacitor exceeds the first reference voltage and a second binary value when the reference voltage is below the second reference voltage; one of the first and second binary values causing charging of the capacitor and the other causing discharging of the capacitor; and

switch circuitry for switching the reference voltage to the first reference voltage when the charge/discharge signal goes from the first value to the second value and to the second reference voltage when the charge/discharge signal goes from the second value to the first value.

2. The integrated circuit of claim 1, wherein the comparator circuitry includes only one comparator.

3. The integrated circuit of claim 1, wherein the switch circuitry comprises a voltage divider with first, second, and third resistors connected in series, and a switch connected in parallel with the third resistor; the voltage divider having a reference lead between the first and second resistors, the reference lead providing the reference voltage to the comparator circuitry; the voltage divider having a second lead between the second and third resistors, the second lead being connected to the switch; the switch responding to the first binary value of the charge/discharge signal by providing a conductive path parallel to the third resistance and to the second binary value by providing a non-conductive path.

4. The integrated circuit of claim 1, wherein the first binary value of the charge/discharge signal is a higher voltage than the second binary value and in which the first reference voltage is higher than the second reference voltage.

5. The integrated circuit of claim 4, further comprising a charging switch for charging the capacitor if the charge/discharge signal is the first binary value and a discharging switch for discharging the capacitor if the charge/discharge signal is the second binary value.

6. An integrated circuit for providing a variable frequency oscillating signal, comprising:

oscillator circuitry providing alternating charging and discharging subcycles in response to the value of the voltage across a capacitor which is charged through a charging resistance during each charging subcycle, and discharged through a discharging resistance during each discharging subcycle; and

frequency varying circuitry for varying the frequency of the charging and discharging subcycles in response to an upward ramping voltage; the frequency varying circuitry modifying at least one of the charging resistance and the discharging resistance as the ramping voltage rises so that the frequency varies.

7. The integrated circuit of claim 6, wherein the frequency varying circuitry smoothly modifies at least one of the charging resistance and the discharging resistance as the ramping voltage rises so that the frequency varies smoothly.

8. The integrated circuit of claim 6, wherein the frequency varying circuitry does not include a comparator.

9. The integrated circuit of claim 8, wherein the frequency varying circuitry includes a current source for charging the ramping capacitor through a ramping lead; the subcycles having an initial frequency when the current source begins charging the ramping capacitor and having an operating frequency when the current source completes charging the ramping capacitor.

10. The integrated circuit of claim 9, wherein the oscillating signal is provided to a lamp and the initial frequency is a preheat frequency greater than the operating frequency.

11. The integrated circuit of claim 10, wherein the frequency varying circuitry further comprises a switch element that provides a conductive path to charge the capacitor through first and second resistances, respectively, when the ramping voltage is low and that provides a non-conductive path to remove the second charging resistive element from the charging resistance when the ramping voltage is high..

12. The integrated circuit of claim 11, wherein the frequency varying circuitry further includes adjusting circuitry for adjusting the voltage across the ramping capacitor in response to a DC bus voltage; the adjusting circuitry including an adjusting switch that provides a conductive path across the ramping capacitor when the DC bus voltage falls below a threshold.

13. The integrated circuit of claim 12, wherein the adjusting switch has a bus sensing lead for connecting to the DC bus through a first dividing resistance; the frequency varying circuitry further including delay circuitry for connecting the bus sensing lead to the ground lead through a second dividing resistance when the ramping voltage reaches a threshold voltage, thus allowing the adjusting switch to begin responding to the DC bus voltage.

14. The integrated circuit of claim 6, wherein the oscillator circuitry includes:

comparator circuitry for comparing the voltage across the capacitor to a reference voltage and generating a charge/discharge signal in response to the value of the voltage across the capacitor as compared to the reference voltage, wherein the reference voltage is switched between at least two values comprising a first reference voltage and a second reference voltage, and wherein the charge/discharge signal has a first binary value when the voltage across the capacitor exceeds the first reference voltage and a second binary value when the reference voltage is below the second reference voltage; one of the first and second binary values causing charging of the capacitor and the other causing discharging of the capacitor; and

switch circuitry for switching the reference voltage to the first reference voltage when the charge/discharge signal goes from the first value to the second value and to the second reference voltage when the charge/discharge signal goes from the second value to the first value.

15. The integrated circuit of claim 14, wherein the oscillator circuitry includes only one comparator.

16. A ballast control IC comprising an oscillator circuit, a preheat circuit

and a start-up circuit, the oscillator circuit including only one comparator such that a smaller layout space is required and the overall size of the IC is reduced.

17. The ballast control IC as recited in claim 16, wherein the preheat circuit generates a preheat frequency, and wherein the preheat frequency is programmed using an external pre-heat resistor in parallel with a timing resistor, the preheat resistor being gradually disconnected as the ballast control IC enters a run mode following the pre-heat frequency.

18. The ballast control IC as recited in claim 17, wherein the preheat circuit generates a preheat voltage ramp to determine the preheat period, and the preheat voltage ramp is also used as an ignition ramp.

19. The ballast control IC of claim 17, wherein the preheat circuit does not include a comparator.

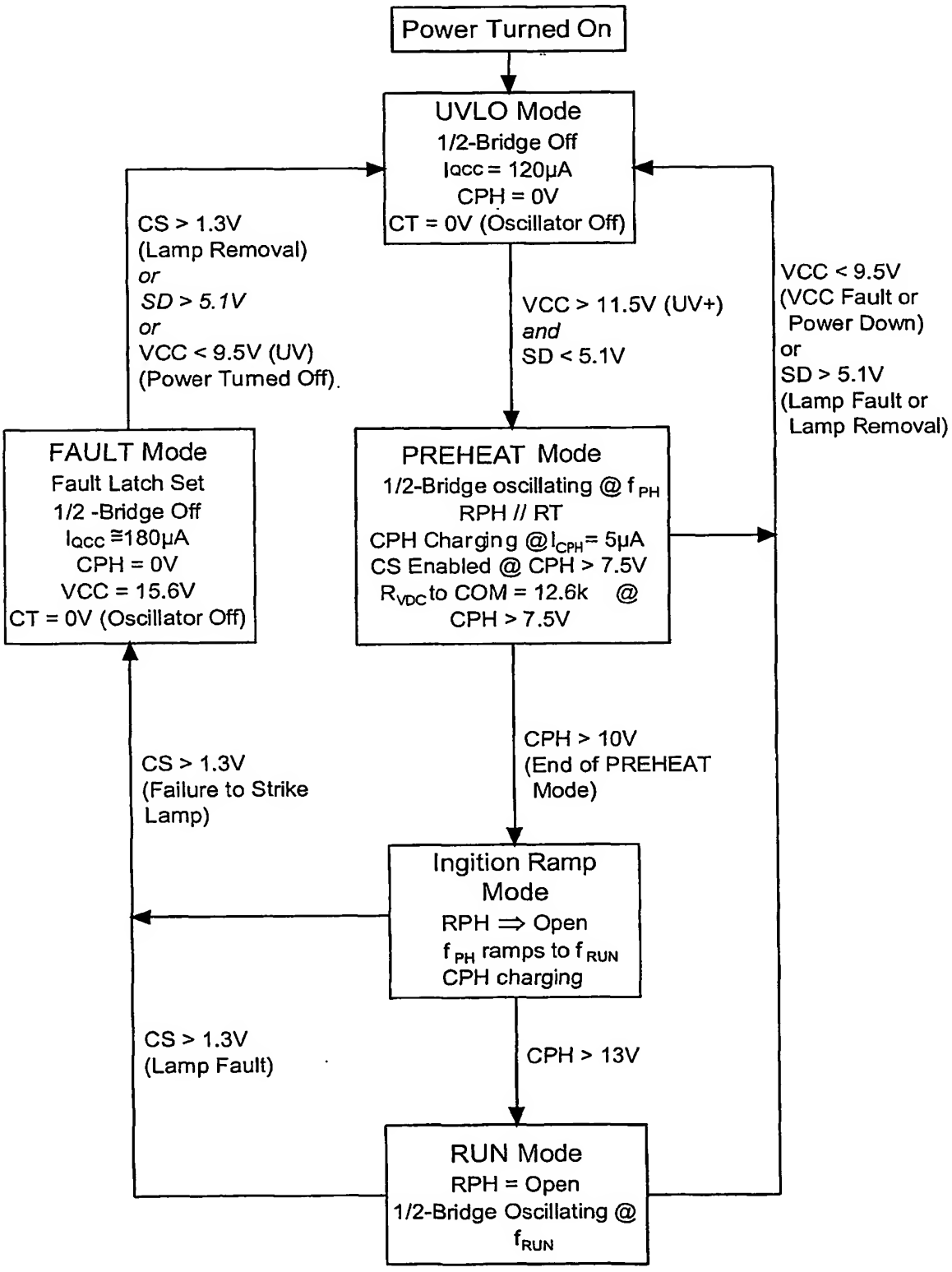

Power Turned On
UVLO Mode
1/2-Bridge Off
Iqcc = 120µA
CPH = 0V
CT = 0V (Oscillator Off)
CS > 1.3V
(Lamp Removal)
or
SD > 5.1V
or
VCC < 9.5V (UV)
(Power Turned Off).
VCC > 11.5V (UV+)
and
SD < 5.1V
VCC < 9.5V
(VCC Fault or
Power Down)
or
SD > 5.1V
(Lamp Fault or
Lamp Removal)
FAULT Mode
Fault Latch Set
1/2 -Bridge Off
Iqcc ≅180µA
CPH = 0V
VCC = 15.6V
CT = 0V (Oscillator Off)
PREHEAT Mode
1/2-Bridge oscillating @ f PH
RPH // RT
CPH Charging @ICPH= 5µA
CS Enabled @ CPH > 7.5V
RVDC to COM = 12.6k @
CPH > 7.5V
CS > 1.3V
(Failure to Strike
Lamp)
CPH > 10V
(End of PREHEAT
Mode)
Ingition Ramp
Mode
RPH ⇒ Open
f PH ramps to f RUN
CPH charging
CS > 1.3V
(Lamp Fault)
CPH > 13V
RUN Mode
RPH = Open
1/2-Bridge Oscillating @
fRUN

FIG. 1

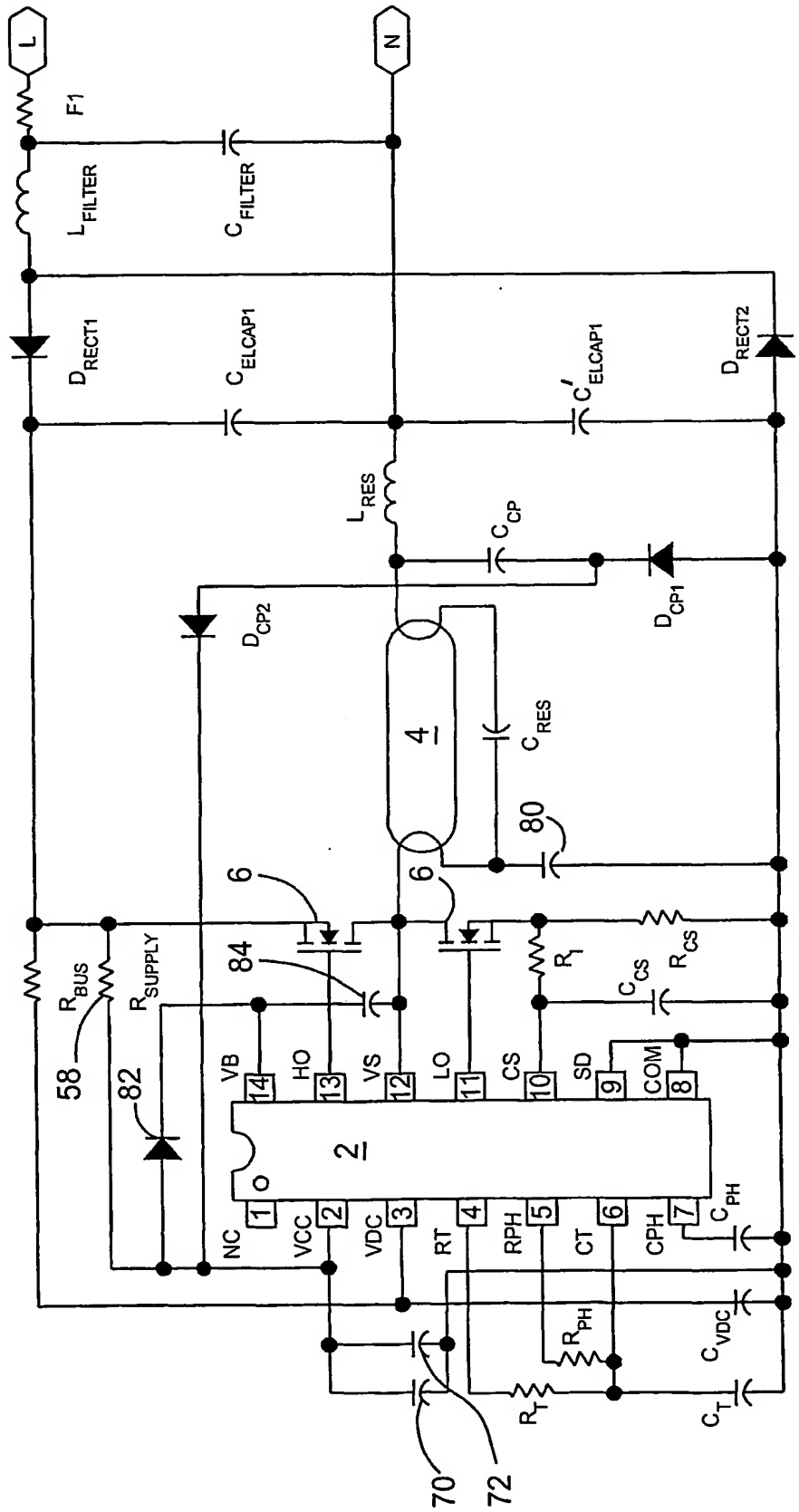

L
N
F1
L_{FILTER}
C_{FILTER}
D_{RECT1}
C_{ELCAP1}
C'_{ELCAP1}
D_{RECT2}
L_{RES}
C_{CP}
D_{CP1}
D_{CP2}
4
C_{RES}
80
6
6
84
R_{BUS}
R_{SUPPLY}
58
82
R_I
R_{CS}
C_{CS}
VB 14
HO 13
VS 12
LO 11
CS 10
SD 9
COM 8
2
NC 1
VCC 2
VDC 3
RT 4
RPH 5
CT 6
CPH 7
C_{PH}
R_{PH}
C_{VDC}
R_T
C_T
70
72

FIG. 2

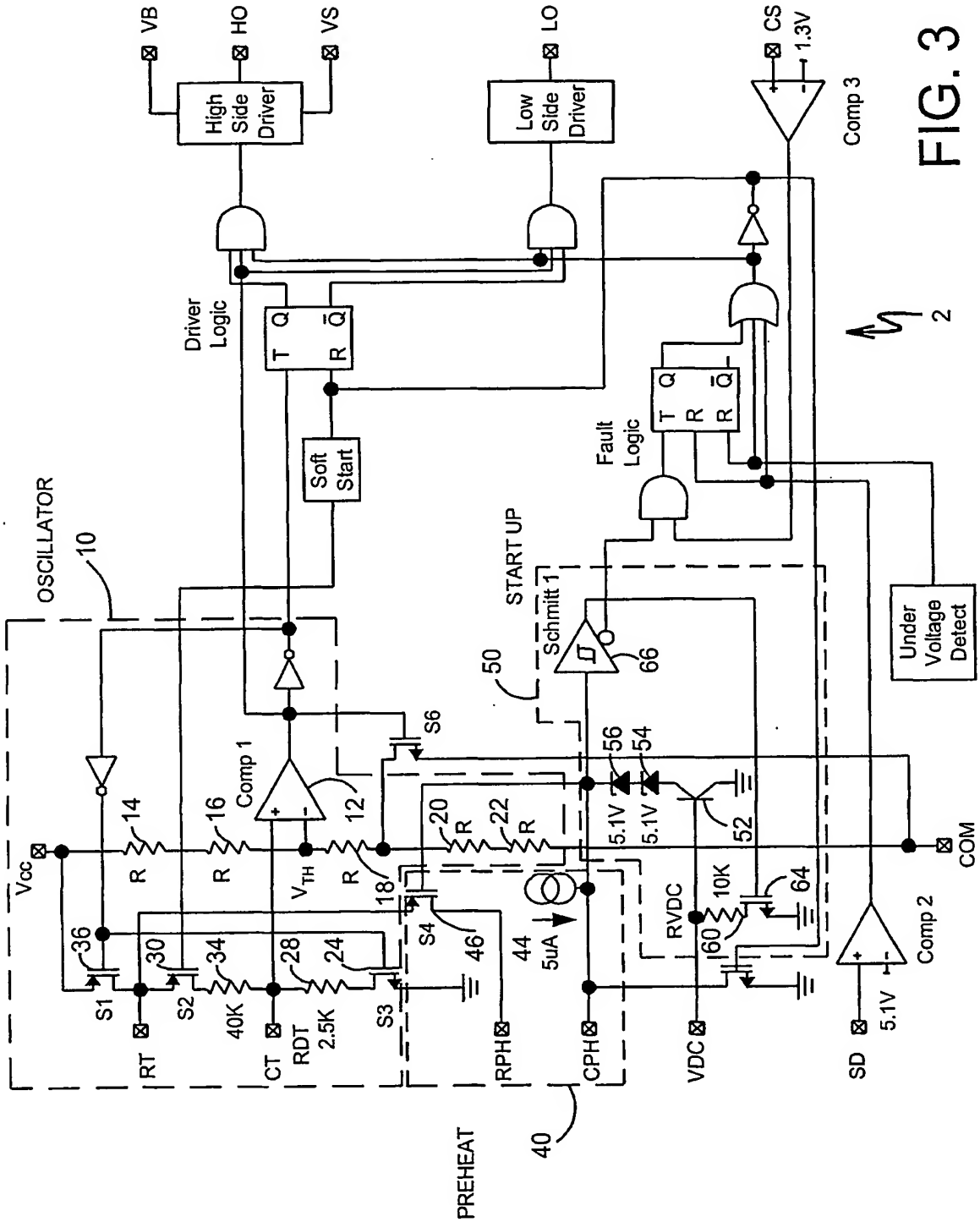

VB
HO
VS
LO
CS
1.3V
High Side Driver
Low Side Driver
Comp 3
Driver Logic
Soft Start
Fault Logic
OSCILLATOR
10
START UP
Schmitt 1
50
66
Under Voltage Detect
S6
Comp 1
12
14
16
20
22
56
54
5.1V
5.1V
52
COM
Vcc
R
R
V_{TH}
R
18
S4
46
44
5uA
RVDC
10K
64
60
Comp 2
36
30
34
28
24
S1
S2
40K
S3
RT
CT
RDT
2.5K
RPH
CPH
VDC
SD
5.1V
PREHEAT
40

FIG. 3

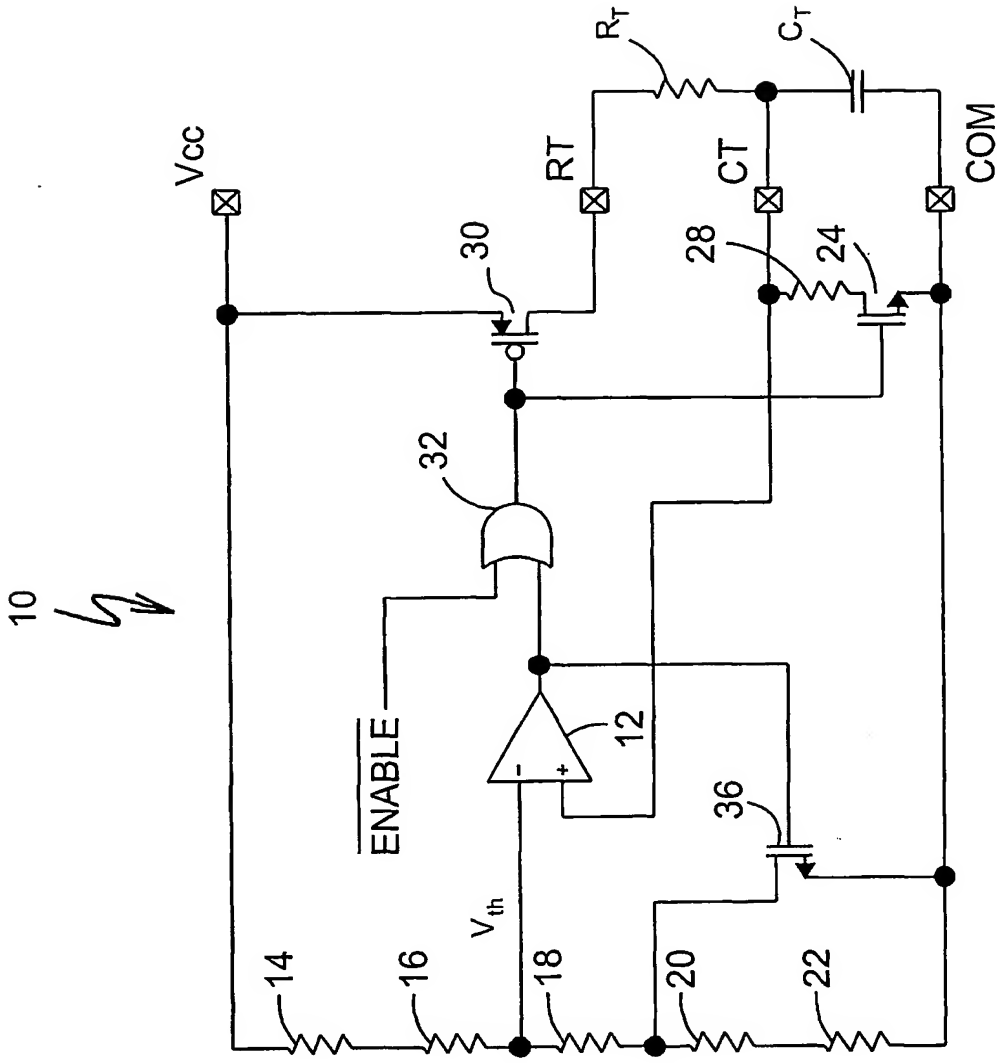


FIG. 4

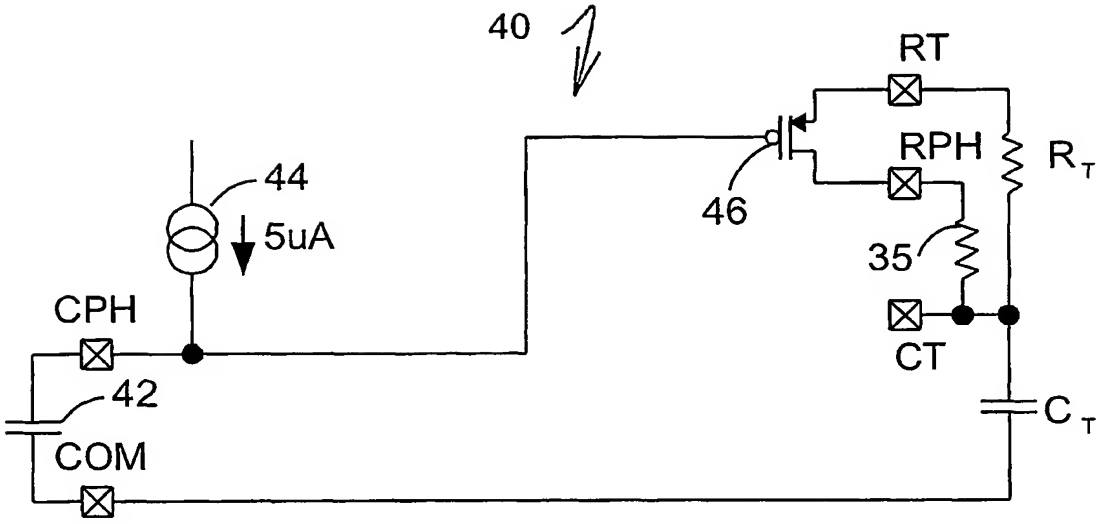

40
RT
RPH
R_T
46
44
5uA
35
CPH
CT
42
C_T
COM

FIG. 5

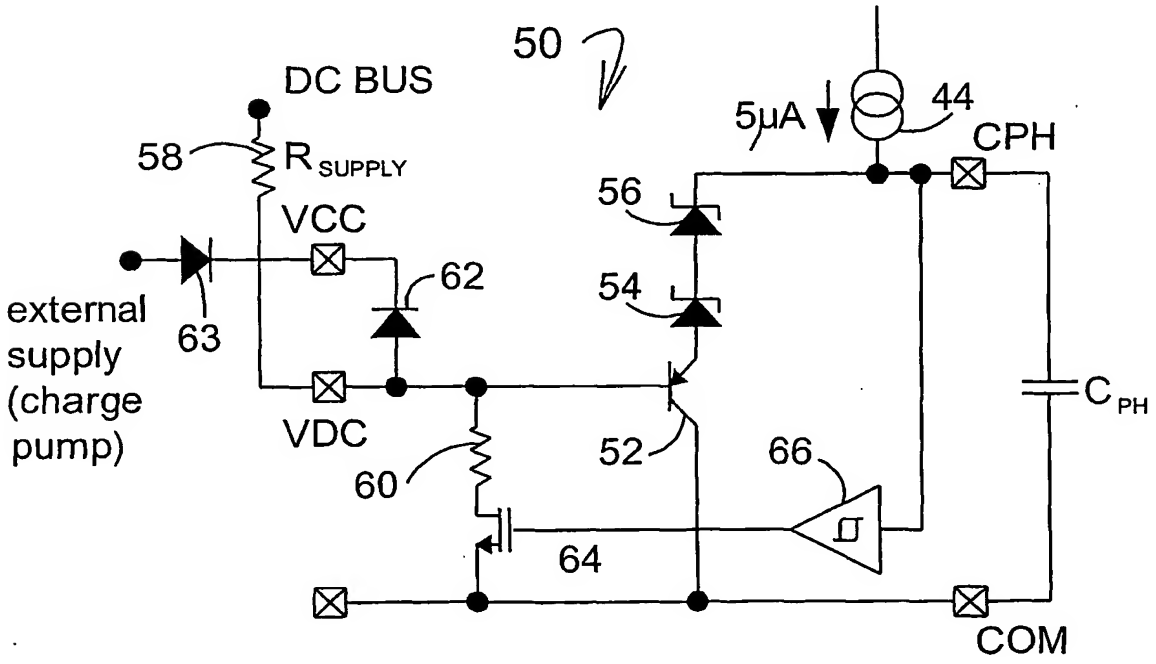

50
DC BUS
5μA
44
CPH
58
R_{SUPPLY}
VCC
56
62
54
external
supply
(charge
pump)
63
VDC
52
66
C_{PH}
60
64
COM

FIG. 6

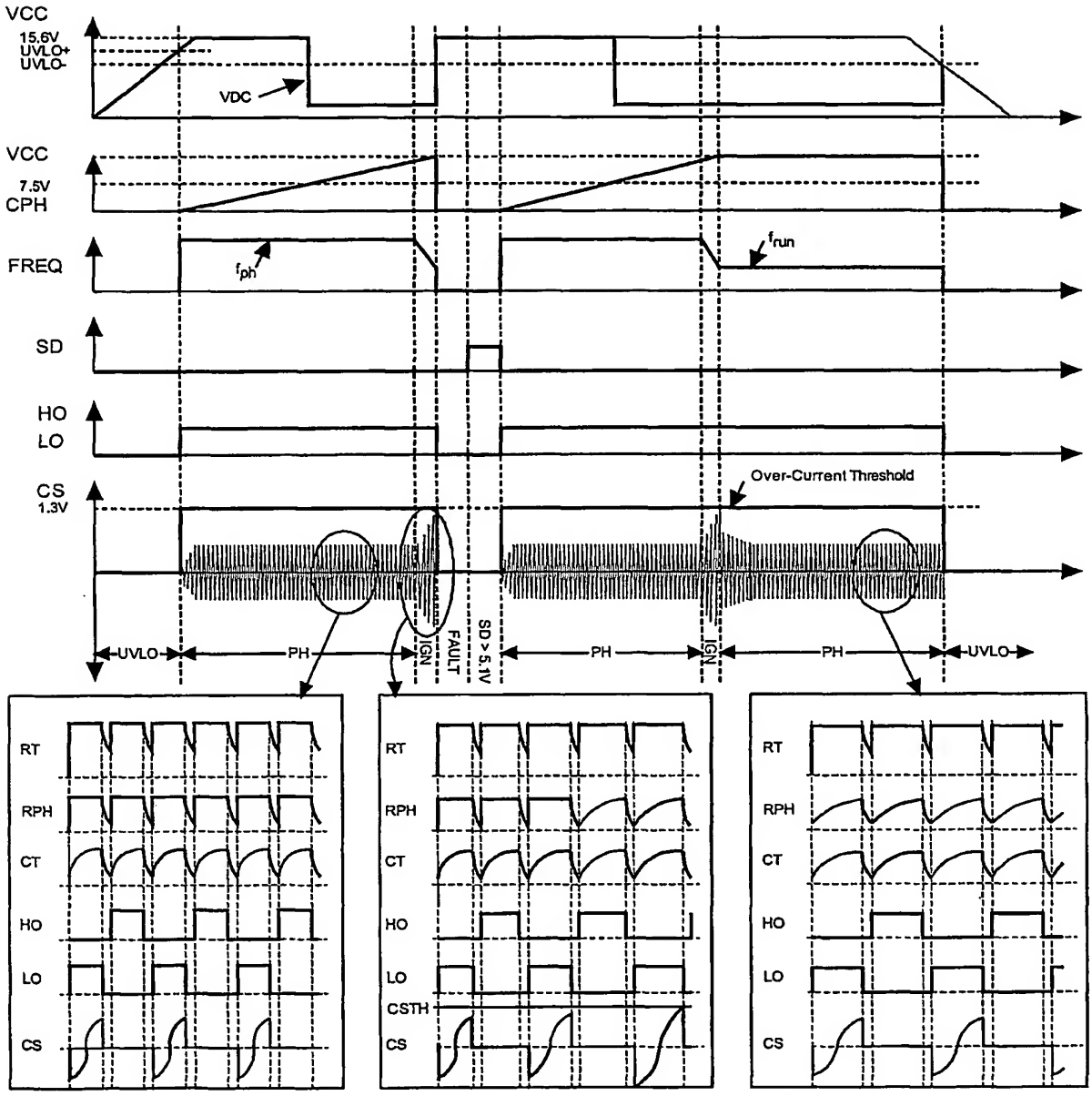

VCC
15.6V
UVLO+
UVLO-
VDC
VCC
7.5V
CPH
FREQ
f_{ph}
f_{run}
SD
HO
LO
CS
1.3V
Over-Current Threshold
UVLO
PH
IGN
FAULT
SD > 5.1V
PH
IGN
PH
UVLO
RT
RPH
CT
HO
LO
CS
RT
RPH
CT
HO
LO
CSTH
CS
RT
RPH
CT
HO
LO
CS

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/19406

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) :G05F 1/100; H05B 37/02
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 315/291, 224, 209R, DIG. 7, 308, 247, 127, DID. 4, DIG. 5; 361/57

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
363/56, 98, 132

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6,031,342 A (RIBARICH et al) 29 February 2000 (29/02/00) entire document.	1-19
Y,P	US 6,211,623 B1 (WILHELM et al) 03 April 2001 (03/04/01) entire document.	1-19
Y	US 5,932,974 A (WOOD) 03 August 1999 (03/08/99) entire document.	1-19
Y	US 6,008,593 A (RIBARICH) 28 December 1999, (28/12/99) entire document.	1-19

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
10 AUGUST 2001	29 AUG 2001
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer CHUC TRAN Telephone No. (703) 306-5984

Form PCT/ISA/210 (second sheet) (July 1998) ★

INTERNATIONAL SEARCH REPORT

Intern application No.
PCT/US01/19406

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

315/291, 224, 209R, DIG. 7, 308, 247, 127, DID. 4, DIG. 5; 361/57